FIG. 2

START

INPUT DEVICE STRUCTURE AND BIAS CONDITION — S201

GENERATE DISCRETE LATTICE POINT — S202

SET BIAS — S203

ANALYZE PHYSICAL EQUATION — S204

CALCULATE CURRENT AT EACH TERMINAL — S205

CALCULATE CARRIER GENERATION/ EXTINCTION SPEED INTEGRATED IN SEMICONDUCTOR REGION — S206

OUTPUT — S207

S208 CHANGE BIAS CONDITION ? YES

NO

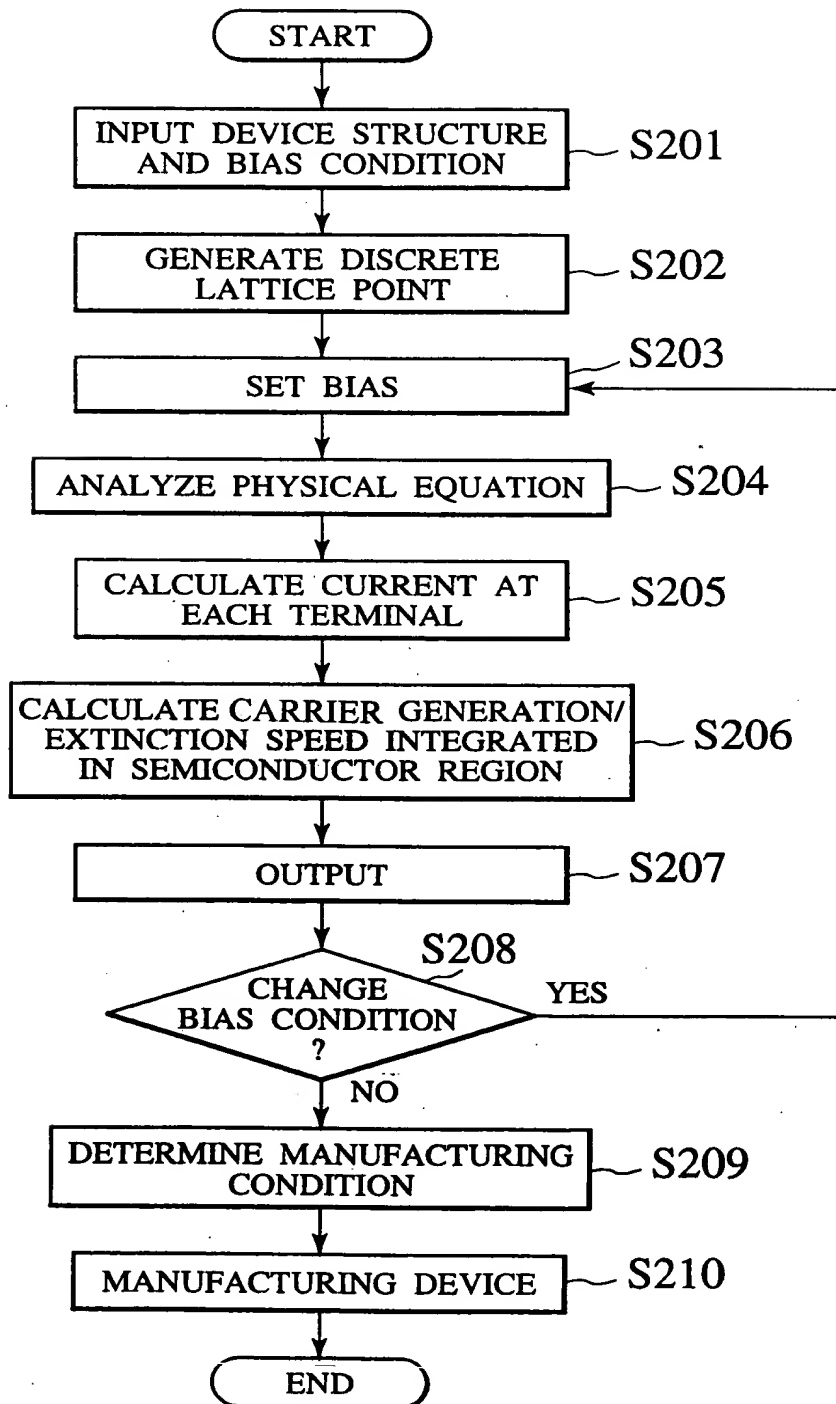DETERMINE MANUFACTURING CONDITION — S209

MANUFACTURING DEVICE — S210

END

PRIOR ART

FIG. 7A $\qquad \dfrac{\delta n}{\delta t} = \dfrac{1}{q} \vec{\nabla} \cdot \vec{J_n} + GR_n$

PRIOR ART

FIG. 7B $\qquad GR_n = GR_{SRHn} + GR_{IIn} + GR_{BBTn}$

FIG. 7C $\qquad A_{SRHn} = \displaystyle\int_{Si} GR_{SRHn} dv$

FIG. 7D $\qquad A_{IIn} = \displaystyle\int_{Si} GR_{IIn} dv$

FIG. 7E $\qquad A_{BBTn} = \displaystyle\int_{Si} GR_{BBTn} dv$

FIG. 7F $\qquad J_{SRHn} = q \displaystyle\int_{Si} GR_{SRHn} dv$

FIG. 7G $\qquad J_{IIn} = q \displaystyle\int_{Si} GR_{IIn} dv$

FIG. 7H $\qquad J_{BBTn} = q \displaystyle\int_{Si} GR_{BBTn} dv$